Low Cost, High Speed Rail-to-Rail Amplifiers

AD8051/AD8052/AD8054

FEATURES

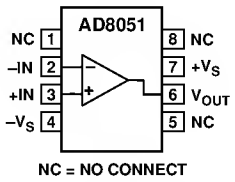
Low Cost Single (AD8051), Dual (AD8052) and Quad (AD8054)
Voltage Feedback Architecture
Fully Specified at +3 V, +5 V and ±5 V Supplies
Single Supply Operation
  Output Swings to Within 25 mV of Either Rail
  Input Voltage Range: –0.2 V to +4 V; V_S = +5 V
High Speed and Fast Settling on +5 V:
  110 MHz –3 dB Bandwidth (G = +1) (AD8051/AD8052)
  150 MHz –3 dB Bandwidth (G = +1) (AD8054)
  145 V/μs Slew Rate
  50 ns Settling Time to 0.1%
Small Packaging
  AD8051 Available in SOT-23-5
  AD8052 Available in microSOIC-8
  AD8054 Available in TSSOP-14
Good Video Specifications (G = +2)
  Gain Flatness of 0.1 dB to 20 MHz; R_L = 150 Ω
  0.03% Differential Gain Error; R_L = 1K
  0.03° Differential Phase Error; R_L = 1K
Low Distortion
  –80 dBc Total Harmonic @ 1 MHz, R_L = 100 Ω
Outstanding Load Drive Capability
  Drives 45 mA, 0.5 V from Supply Rails (AD8051/AD8052)
  Drives 50 pF Capacitive Load (G = +1) (AD8051/AD8052)
Low Power of 2.75 mA/Amplifier (AD8054)
Low Power of 4.4 mA/Amplifier (AD8051/AD8052)

APPLICATIONS

Coax Cable Driver
Active Filters
Video Switchers
A/D Driver
Professional Cameras
CCD Imaging Systems
CD/DVD ROM

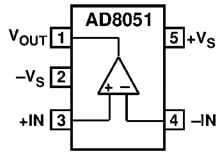
CONNECTION DIAGRAMS
(Top Views)

R-8

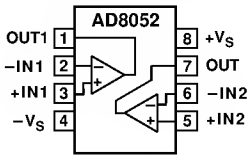


NC = NO CONNECT

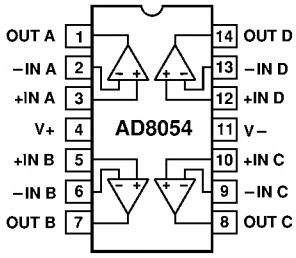
SOT-23-5 (RT)



R-8, microSOIC (RM)



R-14, TSSOP-14 (RU-14)



PRODUCT DESCRIPTION

The AD8051 (single), AD8052 (dual) and AD8054 (quad) are low cost, voltage feedback, high speed amplifiers designed to operate on +3 V, +5 V or ±5 V supplies. They have true single supply capability with an input voltage range extending 200 mV below the negative rail and within 1 V of the positive rail.

Despite their low cost, the AD8051/AD8052/AD8054 provide excellent overall performance and versatility. The output voltage swing extends to within 25 mV of each rail, providing the maximum output dynamic range with excellent overdrive recovery. This makes the AD8051/AD8052/AD8054 useful for video electronics such as cameras, video switchers or any high speed portable equipment. Low distortion and fast settling make them ideal for active filter applications.

The AD8051/AD8052/AD8054 offer low power supply current and can operate on a single +3 V power supply. These features are ideally suited for portable and battery powered applications where size and power are critical.

The wide bandwidth and fast slew rate on a single +5 V supply make these amplifiers useful in many general purpose, high speed applications where dual power supplies of up to ±6 V and single supplies from +3 V to +12 V are needed.

All of this low cost performance is offered in an 8-lead SOIC, along with a tiny SOT-23-5 package (AD8051), a microSOIC package (AD8052) and a TSSOP-14 (AD8054).

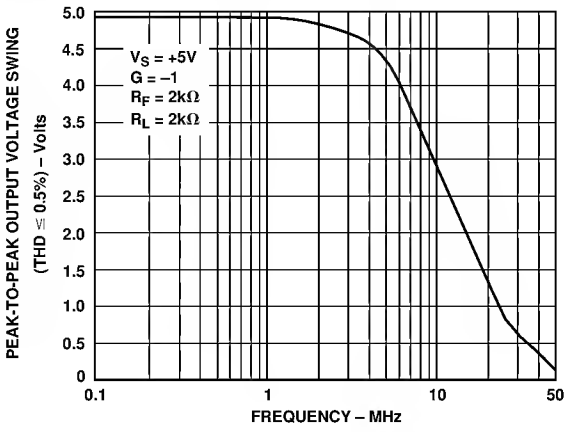


Figure 1. Low Distortion Rail-to-Rail Output Swing

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD8051/AD8052/AD8054– SPECIFICATIONS (@ T_A = +25°C, V_S = +5 V, R_L = 2 kΩ to +2.5 V, unless otherwise noted)

Parameter	Conditions	AD8051A/AD8052A Min	AD8051A/AD8052A Typ	AD8051A/AD8052A Max	AD8054A Min	AD8054A Typ	AD8054A Max	Units
DYNAMIC PERFORMANCE								
–3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	70	110		80	150		MHz
	G = –1, +2, V_O = 0.2 V p-p		50			60		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω to +2.5 V, R_F = 806 Ω for AD8051A/AD8052A		20					MHz
	R_F = 200 Ω for AD8054A					12		MHz
Slew Rate	G = –1, V_O = 2 V Step	100	145		140	170		V/µs
Full Power Response	G = +1, V_O = 2 V p-p		35			45		MHz
Settling Time to 0.1%	G = –1, V_O = 2 V Step		50			40		ns
NOISE/DISTORTION PERFORMANCE								
Total Harmonic Distortion[1]	f_C = 5 MHz, V_O = 2 V p-p, G = +2		–67			–68		dB
Input Voltage Noise	f = 10 kHz		16			16		nV/√Hz
Input Current Noise	f = 10 kHz		850			850		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to +2.5 V		0.09			0.07		%
	R_L = 1 kΩ to +2.5 V		0.03			0.02		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to +2.5 V		0.19			0.26		Degrees
	R_L = 1 kΩ to +2.5 V		0.03			0.05		Degrees
Crosstalk	f = 5 MHz, G = +2		–60			–60		dB
DC PERFORMANCE								
Input Offset Voltage			1.7	10		1.7	12	mV
	T_{MIN}–T_{MAX}			25			30	mV
Offset Drift			10			15		µV/°C
Input Bias Current			1.4	2.5		2	4.5	µA
	T_{MIN}–T_{MAX}			3.25			4.5	µA
Input Offset Current			0.1	0.75		0.2	1.2	µA
Open-Loop Gain	R_L = 2 kΩ to +2.5 V	86	98		82	98		dB
	T_{MIN}–T_{MAX}		96			96		dB
	R_L = 150 Ω to +2.5 V	76	82		74	82		dB
	T_{MIN}–T_{MAX}		78			78		dB
INPUT CHARACTERISTICS								
Input Resistance			290			300		kΩ
Input Capacitance			1.4			1.5		pF
Input Common-Mode Voltage Range			–0.2 to 4			–0.2 to 4		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to +3.5 V	72	88		70	86		dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L = 10 kΩ to +2.5 V		0.015 to 4.985			0.03 to 4.975		V
	R_L = 2 kΩ to +2.5 V	0.1 to 4.9	0.025 to 4.975		0.125 to 4.875	0.05 to 4.95		V
	R_L = 150 Ω to +2.5 V	0.3 to 4.625	0.2 to 4.8		0.55 to 4.4	0.25 to 4.65		V
Output Current	V_{OUT} = 0.5 V to +4.5 V		45			30		mA
	T_{MIN}–T_{MAX}		45			30		mA
Short Circuit Current	Sourcing		80			45		mA
	Sinking		130			85		mA
Capacitive Load Drive	G = +1 (AD8051/AD8052)		50					pF
	G = +2 (AD8054)					40		pF
POWER SUPPLY								
Operating Range		3		12	3		12	V
Quiescent Current/Amplifier			4.4	5		2.75	3.275	mA
Power Supply Rejection Ratio	ΔV_S = ±1 V	70	80		68	80		dB
OPERATING TEMPERATURE RANGE		–40		+85	–40		+85	°C

NOTE
[1]Refer to Figure 15.

Specifications subject to change without notice.

SPECIFICATIONS (@ T_A = +25°C, V_S = +3 V, R_L = 2 kΩ to +1.5 V, unless otherwise noted)

Parameter	Conditions	AD8051A/AD8052A Min	AD8051A/AD8052A Typ	AD8051A/AD8052A Max	AD8054A Min	AD8054A Typ	AD8054A Max	Units
DYNAMIC PERFORMANCE								
–3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	70	110		80	135		MHz
	G = –1, +2, V_O = 0.2 V p-p		50			65		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω to 2.5 V,							
	R_F = 402 Ω for AD8051A/AD8052A		17					MHz
	R_F = 200 Ω for AD8054A					10		MHz
Slew Rate	G = –1, V_O = 2 V Step	90	135		110	150		V/µs
Full Power Response	G = +1, V_O = 1 V p-p		65			85		MHz
Settling Time to 0.1%	G = –1, V_O = 2 V Step		55			55		ns
NOISE/DISTORTION PERFORMANCE								
Total Harmonic Distortion[1]	f_C = 5 MHz, V_O = 2 V p-p,							
	G = –1, R_L = 100 Ω to +1.5 V		–47			–48		dB
Input Voltage Noise	f = 10 kHz		16			16		nV/√Hz
Input Current Noise	f = 10 kHz		600			600		fA/√Hz
Differential Gain Error (NTSC)	G = +2, V_{CM} = +1 V							
	R_L = 150 Ω to +1.5 V,		0.11			0.13		%
	R_L = 1 kΩ to +1.5 V		0.09			0.09		%
Differential Phase Error (NTSC)	G = +2, V_{CM} = +1 V							
	R_L = 150 Ω to +1.5 V		0.24			0.3		Degrees
	R_L = 1 k Ω to +1.5 V		0.10			0.1		Degrees
Crosstalk	f = 5 MHz, G = +2		–60			–60		dB
DC PERFORMANCE								
Input Offset Voltage			1.6	10		1.6	12	mV
	T_{MIN}–T_{MAX}			25			30	mV
Offset Drift			10			15		µV/°C
Input Bias Current			1.3	2.6		2	4.5	µA
	T_{MIN}–T_{MAX}			3.25			4.5	µA
Input Offset Current			0.15	0.8		0.2	1.2	µA
Open-Loop Gain	R_L = 2 kΩ	80	96		80	96		dB
	T_{MIN}–T_{MAX}		94			94		dB
	R_L = 150 Ω	74	82		72	80		dB
	T_{MIN}–T_{MAX}		76			76		dB
INPUT CHARACTERISTICS								
Input Resistance			290			300		kΩ
Input Capacitance			1.4			1.5		pF
Input Common-Mode Voltage Range			–0.2 to 2			–0.2 to 2		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1.5 V	72	88		70	86		dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L = 10 kΩ to +1.5 V		0.01 to 2.99			0.025 to 2.98		V
	R_L = 2 kΩ to +1.5 V	0.075 to 2.9	0.02 to 2.98		0.1 to 2.9	0.35 to 2.965		V
	R_L = 150 Ω to +1.5 V	0.2 to 2.75	0.125 to 2.875		0.35 to 2.55	0.15 to 2.75		V
Output Current	V_{OUT} = 0.5 V to +2.5 V		45			25		mA
	T_{MIN}–T_{MAX}		45			25		mA
Short Circuit Current	Sourcing		60			30		mA
	Sinking		90			50		mA
Capacitive Load Drive	G = +1 (AD8051/AD8052)		45					pF
	G = +2 (AD8054)					35		pF
POWER SUPPLY								
Operating Range		3		12	3		12	V
Quiescent Current/Amplifier			4.2	4.8		2.625	3.125	mA
Power Supply Rejection Ratio	ΔV_S = +0.5 V	68	80		68	80		dB
OPERATING TEMPERATURE RANGE		–40		+85	–40		+85	°C

NOTE

[1]Refer to Figure 15.

Specifications subject to change without notice.

AD8051/AD8052/AD8054- SPECIFICATIONS (@ T_A = +25°C, V_S = ±5 V, R_L = 2 kΩ to Ground, unless otherwise noted)

Parameter	Conditions	AD8051A/AD8052A Min	AD8051A/AD8052A Typ	AD8051A/AD8052A Max	AD8054A Min	AD8054A Typ	AD8054A Max	Units
DYNAMIC PERFORMANCE								
–3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	70	110		85	160		MHz
	G = –1, +2, V_O = 0.2 V p-p		50			65		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω,							
	R_F = 1.1 kΩ for AD8051A/AD8052A		20					MHz
	R_F = 200 Ω for AD8054A					15		MHz
Slew Rate	G = –1, V_O = 2 V Step	105	170		150	190		V/µs
Full Power Response	G = +1, V_O = 2 V p-p		40			50		MHz
Settling Time to 0.1%	G = –1, V_O = 2 V Step		50			40		ns
NOISE/DISTORTION PERFORMANCE								
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, G = +2		–71			–72		dB
Input Voltage Noise	f = 10 kHz		16			16		nV/√Hz
Input Current Noise	f = 10 kHz		900			900		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω		0.02			0.06		%
	R_L = 1 kΩ		0.02			0.02		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω		0.11			0.15		Degrees
	R_L = 1 kΩ		0.02			0.03		Degrees
Crosstalk	f = 5 MHz, G = +2		–60			–60		dB
DC PERFORMANCE								
Input Offset Voltage			1.8	11		1.8	13	mV
	T_{MIN}–T_{MAX}			27			32	mV
Offset Drift			10			15		µV/°C
Input Bias Current			1.4	2.6		2	4.5	µA
	T_{MIN}–T_{MAX}			3.5			4.5	µA
Input Offset Current			0.1	0.75		0.2	1.2	µA
Open-Loop Gain	R_L = 2 kΩ	88	96		84	96		dB
	T_{MIN}–T_{MAX}		96			96		dB
	R_L = 150 Ω	78	82		76	82		dB
	T_{MIN}–T_{MAX}		80			80		dB
INPUT CHARACTERISTICS								
Input Resistance			290			300		kΩ
Input Capacitance			1.4			1.5		pF
Input Common-Mode Voltage Range			–5.2 to 4			–5.2 to 4		V
Common-Mode Rejection Ratio	V_{CM} = –5 V to +3.5 V	72	88		70	86		dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L = 10 kΩ		–4.98 to +4.98			–4.97 to +4.97		V
	R_L = 2 kΩ	–4.85 to +4.85	–4.97 to +4.97		–4.8 to +4.8	–4.9 to +4.9		V
	R_L = 150 Ω	–4.45 to +4.3	–4.6 to +4.6		–4.0 to +3.8	–4.5 to +4.5		V
Output Current	V_{OUT} = –4.5 V to +4.5 V		45			30		mA
	T_{MIN}–T_{MAX}		45			30		mA
Short Circuit Current	Sourcing		100			60		mA
	Sinking		160			100		mA
Capacitive Load Drive	G = +1 (AD8051/AD8052)		50					pF
	G = +2 (AD8054)					40		pF
POWER SUPPLY								
Operating Range		3		12	3		12	V
Quiescent Current/Amplifier			4.8	5.5		2.875	3.4	mA
Power Supply Rejection Ratio	ΔV_S = ±1 V	68	80		68	80		dB
OPERATING TEMPERATURE RANGE		–40		+85	–40		+85	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.6 V
Internal Power Dissipation[2]
Small Outline Package (R) . . . Observe Power Derating Curves
SOT-23-5 Package . . . . . Observe Power Derating Curves
microSOIC Package . . . . . Observe Power Derating Curves
TSSOP-14 Package . . . . . Observe Power Derating Curves
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±2.5 V
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range R . . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Lead SOIC: θ_{JA} = 160°C/Watt
5-Lead SOT-23-5: θ_{JA} = 240°C/Watt
8-Lead microSOIC: θ_{JA} = 200°C/Watt
14-Lead SOIC: θ_{JA} = 120°C/Watt
14-Lead TSSOP: θ_{JA} = 180°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options*
AD8051AR	–40°C to +85°C	8-Lead SOIC	R-8
AD8051ART	–40°C to +85°C	5-Lead SOT-23-5	RT-5
AD8052AR	–40°C to +85°C	8-Lead SOIC	R-8
AD8052ARM	–40°C to +85°C	8-Lead microSOIC	RM-08
AD8054AR	–40°C to +85°C	14-Lead SOIC	R-14
AD8054ARU	–40°C to +85°C	14-Lead microSOIC	RU-14

*R = Small Outline; RM = Micro Small Outline; RT = Surface Mount; RU = TSSOP .

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8051/AD8052/AD8054 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8051/AD8052/AD8054 are internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

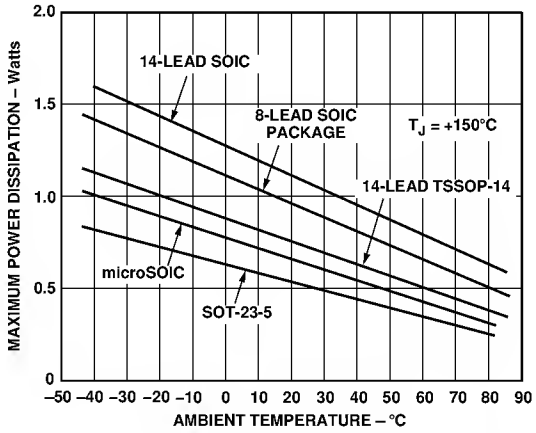


Figure 2. Plot of Maximum Power Dissipation vs. Temperature for AD8051/AD8052/AD8054

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8051/AD8052/AD8054 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

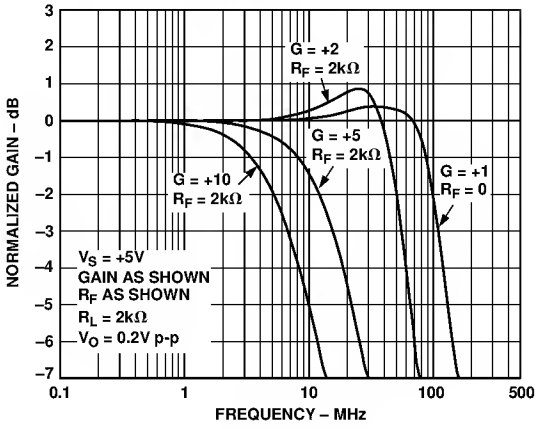


Figure 3. AD8051/AD8052 Frequency Response vs. Closed-Loop Gain; V_S = ±5 V

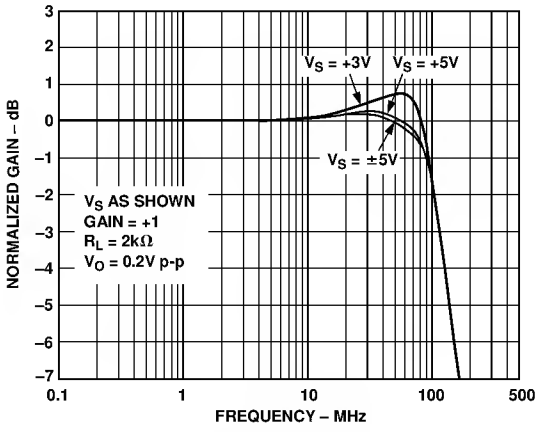


Figure 4. AD8051/AD8052 Closed-Loop Frequency Response vs. Supply

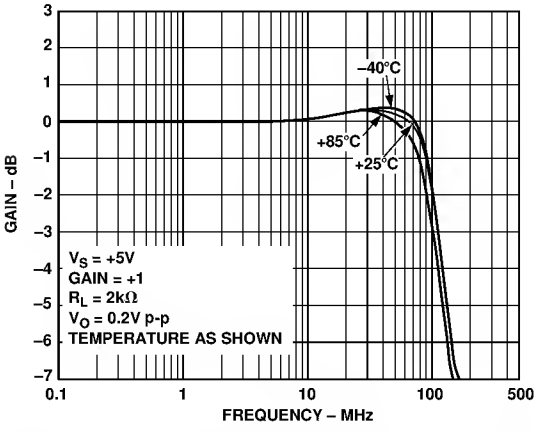


Figure 5. AD8051/AD8052 Closed-Loop Frequency Response vs. Temperature

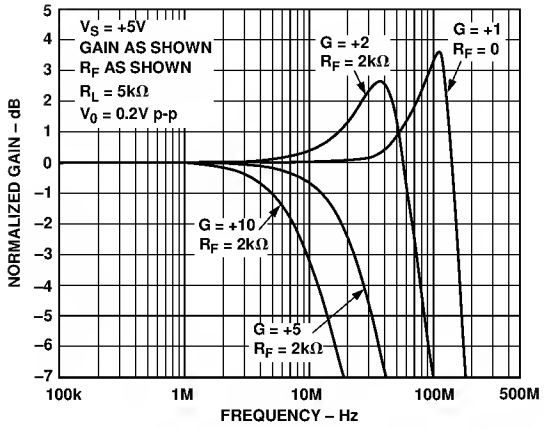


Figure 6. AD8054 Frequency Response vs. Closed-Loop Gain; V_S = ±5 V

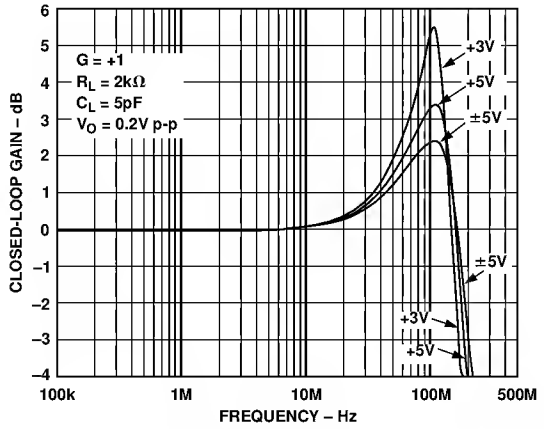


Figure 7. AD8054 Closed-Loop Frequency Response vs. Supply

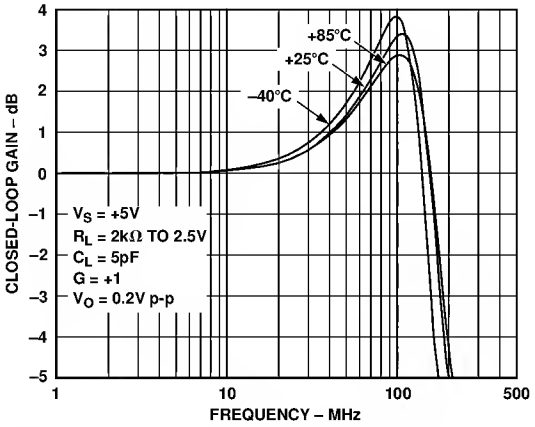


Figure 8. AD8054 Closed-Loop Frequency Response vs. Temperature

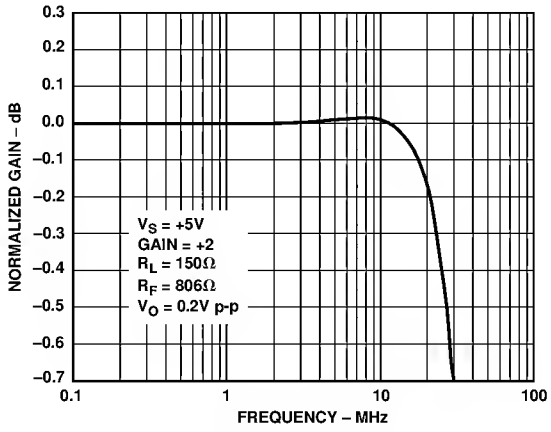


Figure 9. AD8051/AD8052 0.1 dB Gain Flatness; G = +2

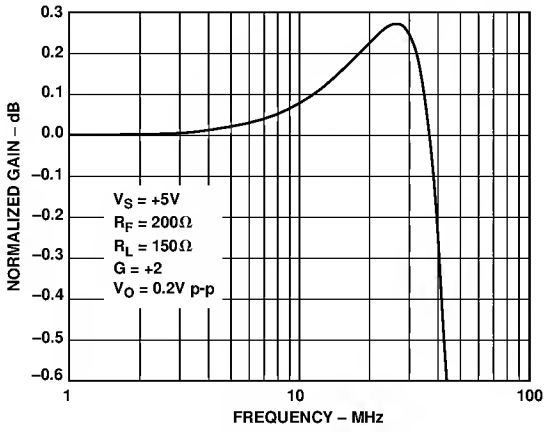


Figure 12. AD8054 0.1 dB Gain Flatness; G = +2

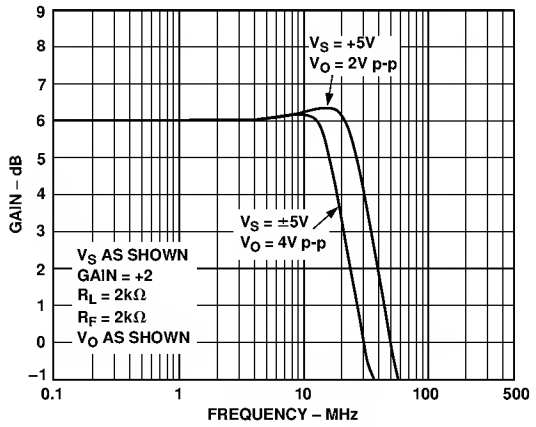


Figure 10. AD8051/AD8052 Large Signal Frequency Response; G = +2

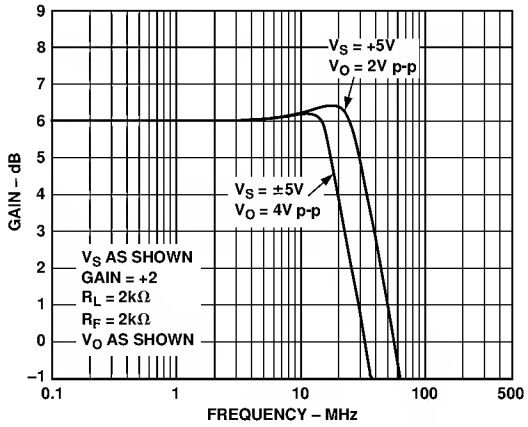


Figure 13. AD8054 Large Signal Frequency Response; G = +2

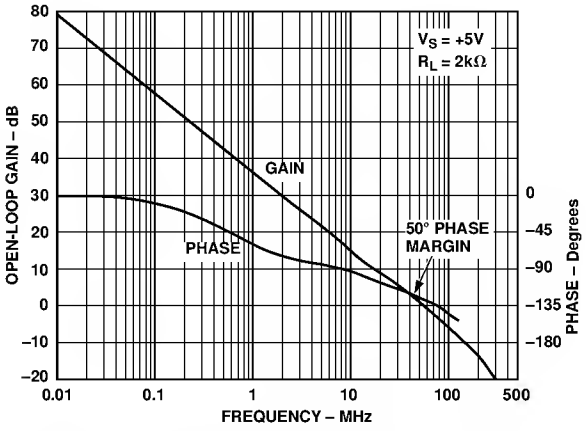


Figure 11. AD8051/AD8052 Open-Loop Gain and Phase vs. Frequency

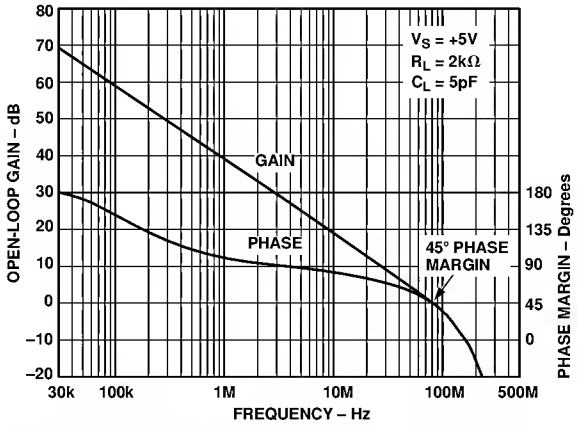


Figure 14. AD8054 Open-Loop Gain and Phase Margin vs. Frequency

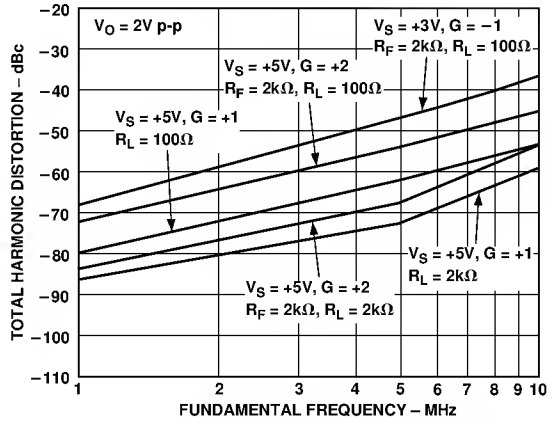


Figure 15. Total Harmonic Distortion

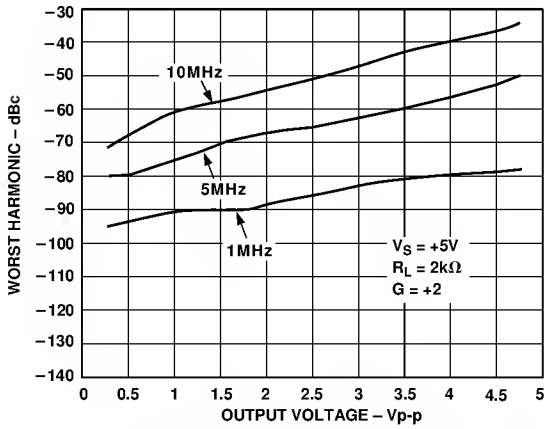


Figure 16. Worst Harmonic vs. Output Voltage

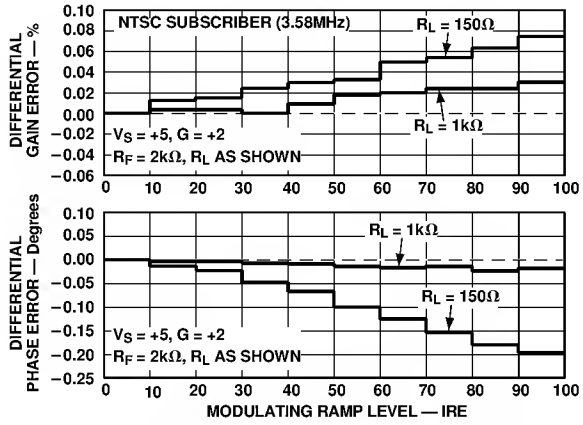


Figure 17. AD8051/AD8052 Differential Gain and Phase Errors

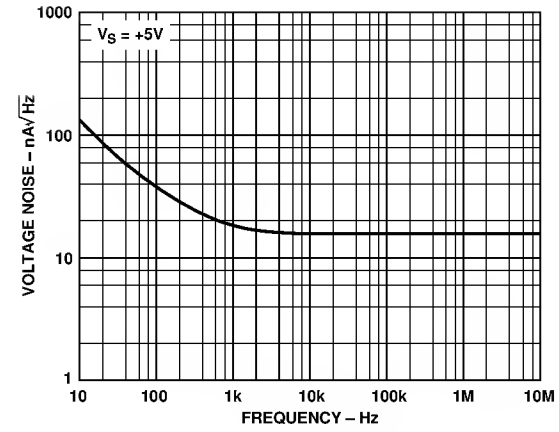


Figure 18. Input Voltage Noise vs. Frequency

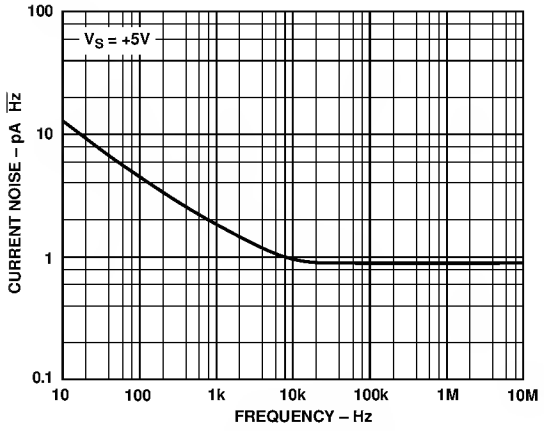


Figure 19. Input Current Noise vs. Frequency

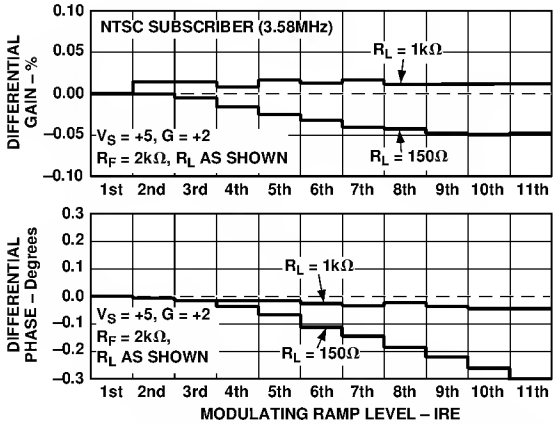


Figure 20. AD8054 Differential Gain and Phase Errors

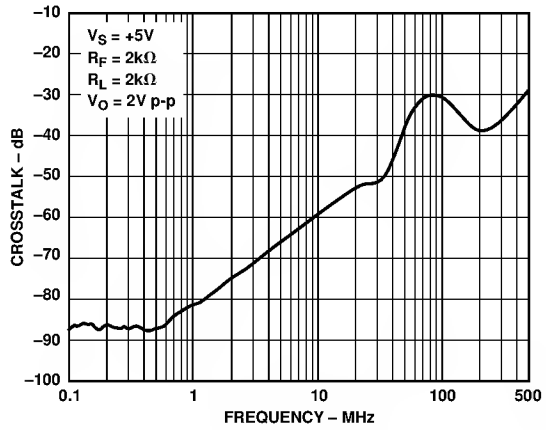


Figure 21. AD8052 Crosstalk (Output-to-Output) vs. Frequency

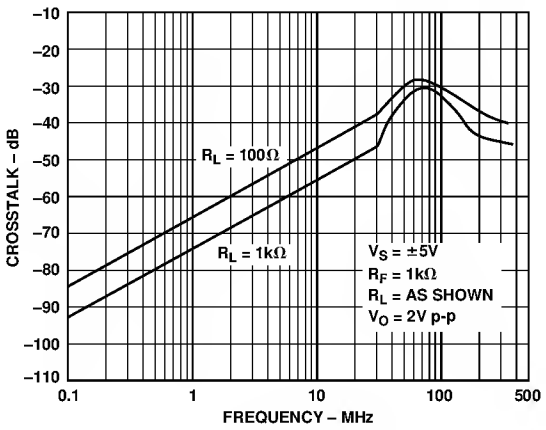


Figure 24. AD8054 Crosstalk (Output-to-Output) vs. Frequency

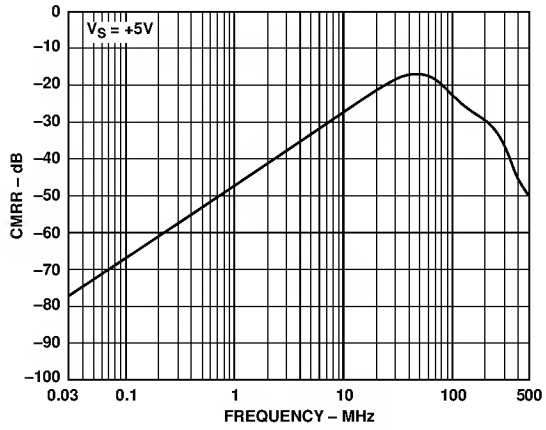


Figure 22. CMRR vs. Frequency

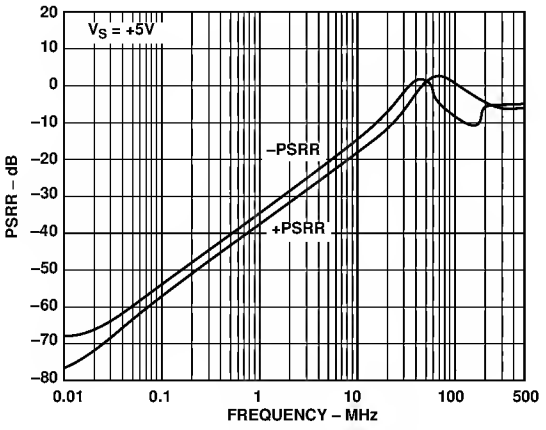


Figure 25. PSRR vs. Frequency

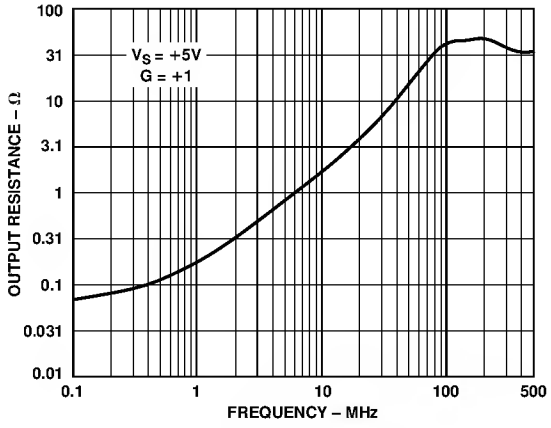


Figure 23. Closed Loop Output Resistance vs. Frequency

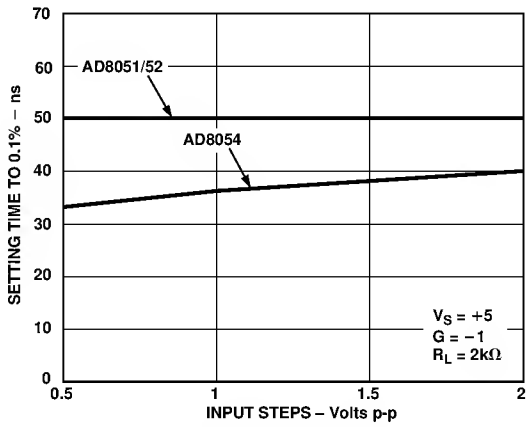


Figure 26. Settling Time vs. Input Step

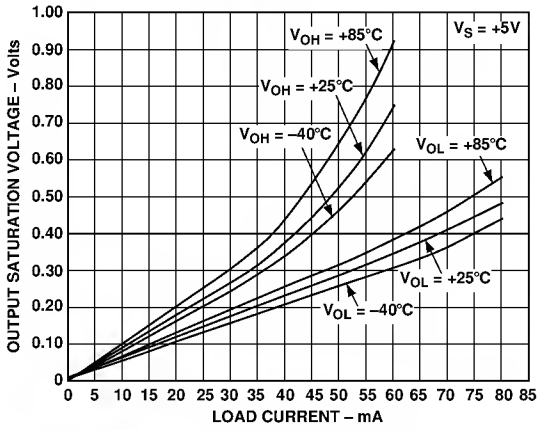


Figure 27. AD8051/AD8052 Output Saturation Voltage vs. Load Current

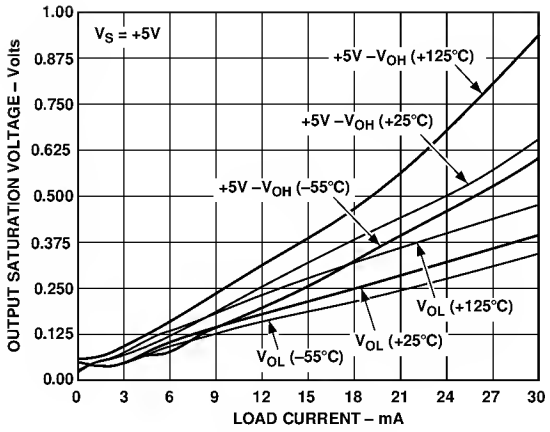


Figure 29. AD8054 Output Saturation Voltage vs. Load Current

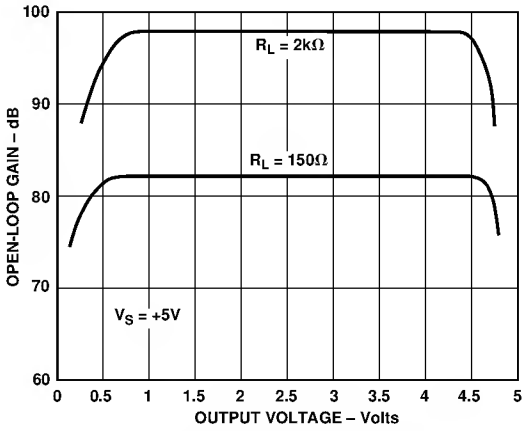


Figure 28. Open-Loop Gain vs. Output Voltage

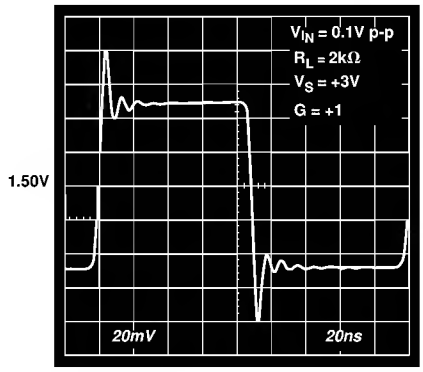


Figure 30. 100 mV Step Response, G = +1

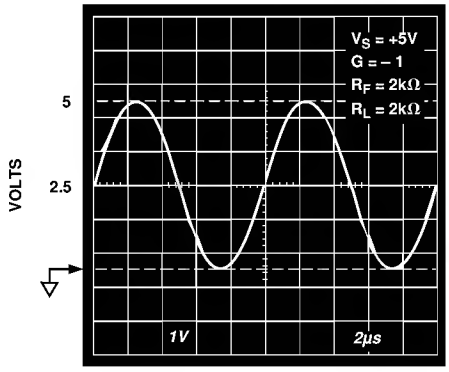


Figure 33. Output Swing; G = –1, R_L = +2 kΩ

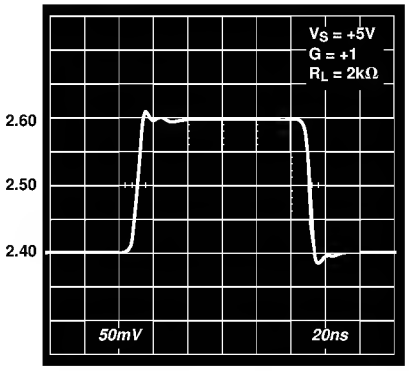


Figure 31. AD8051/AD8052 200 mV Step Response; V_S = +5 V, G = +1

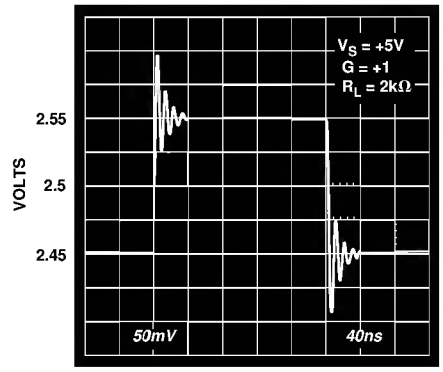


Figure 34. AD8054 100 mV Step Response; V_S = +5 V, G = +1

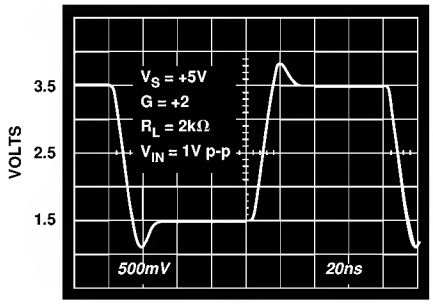


Figure 32. Large Signal Step Response; V_S = +5 V, G = +2

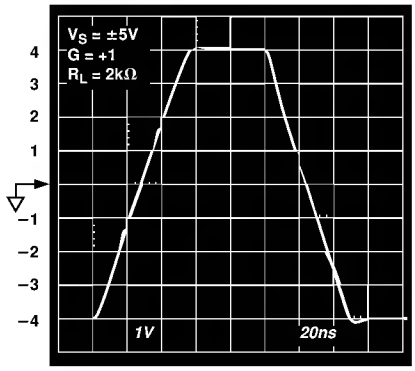


Figure 35. Large Signal Step Response; V_S = ±5 V, G = +1

Overdrive Recovery

Overdrive of an amplifier occurs when the output and/or input range are exceeded. The amplifier must recover from this overdrive condition. As shown in Figure 36, the AD8051/AD8052/AD8054 recovers within 60 ns from negative overdrive and within 45 ns from positive overdrive.

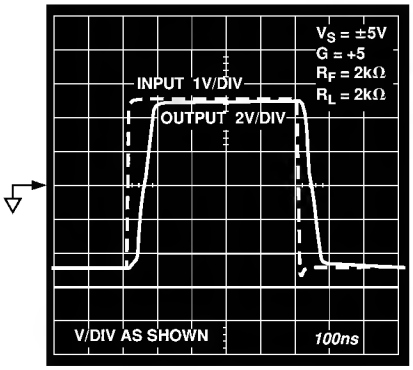


Figure 36. Overdrive Recovery

Driving Capacitive Loads

Consider the AD8051/AD8052 in a closed-loop gain of +1 with $+V_S$ = 5 V and a load of 2 kΩ in parallel with 50 pF. Figures 37 and 38 show its frequency and time domain responses, respectively, to a small-signal excitation. The capacitive load drive of the AD8051/AD8052/AD8054 can be increased by adding a low valued resistor in series with the load. Figures 39 and 40 show the effect of a series resistor on capacitive drive for varying voltage gains. As the closed-loop gain is increased, the larger phase margin allows for larger capacitive loads with less peaking. Adding a series resistor with lower closed-loop gains accomplishes the same effect. For large capacitive loads, the frequency response of the amplifier will be dominated by the roll-off of the series resistor and the load capacitance.

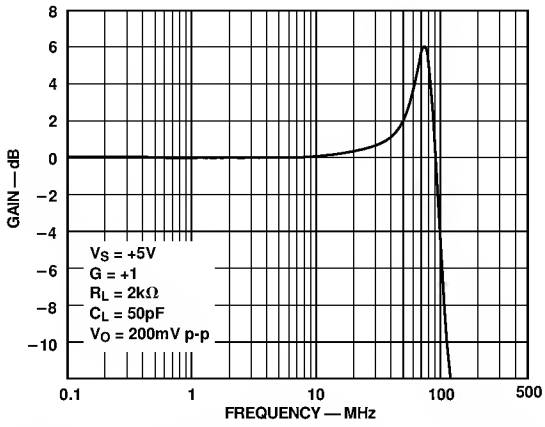


Figure 37. AD8051/AD8052 Closed-Loop Frequency Response: C_L = 50 pF

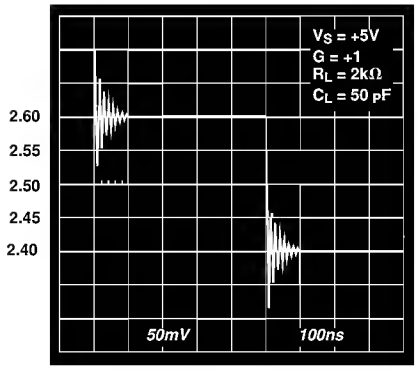


Figure 38. AD8051/AD8052 200 mV Step Response: C_L = 50 pF

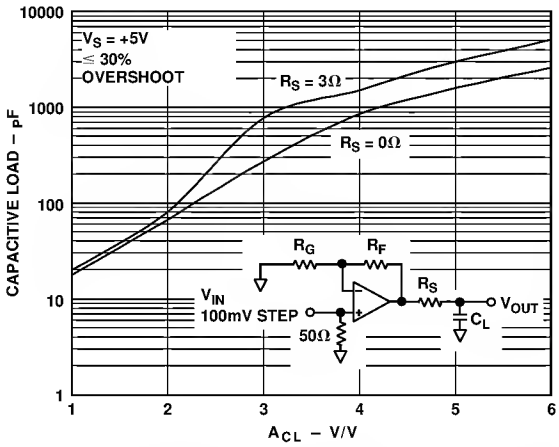


Figure 39. AD8051/AD8052 Capacitive Load Drive vs. Closed-Loop Gain

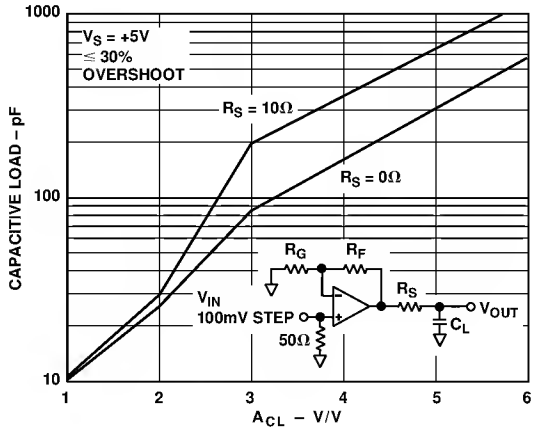


Figure 40. AD8054 Capacitive Load Drive vs. Closed-Loop Gain

Circuit Description

The AD8051/AD8052/AD8054 is fabricated on Analog Devices' proprietary eXtra-Fast Complementary Bipolar (XFCB) process, which enables the construction of PNP and NPN transistors with similar f_Ts in the 2 GHz–4 GHz region. The process is dielectrically isolated to eliminate the parasitic and latch-up

problems caused by junction isolation. These features allow the construction of high frequency, low distortion amplifiers with low supply currents. This design uses a differential output input stage to maximize bandwidth and headroom (see Figure 1). The smaller signal swings required on the first stage outputs (nodes S1P, S1N) reduce the effect of nonlinear currents due to junction capacitances and improve the distortion performance. With this design harmonic distortion of –80 dBc @ 1 MHz into 100 Ω with V_{OUT} = 2 V p-p (Gain = +1) on a single 5 volt supply is achieved.

The inputs of the device can handle voltages from –0.2 V below the negative rail to within 1 V of the positive rail. Exceeding these values will not cause phase reversal; however, the input ESD devices will begin to conduct if the input voltages exceed the rails by greater than 0.5 V. During this overdrive condition, the output stays at the rail.

The rail-to-rail output range of the AD8051/AD8052/AD8054 is provided by a complementary common-emitter output stage. High output drive capability is provided by injecting all output stage predriver currents directly into the bases of the output devices Q8 and Q36. Biasing of Q8 and Q36 is accomplished by I8 and I5, along with a common-mode feedback loop (not shown). This circuit topology allows the AD8051/AD8052 to drive 45 mA of output current and the AD8054 to drive 30 mA of output current with the outputs within 0.5 V of the supply rails.

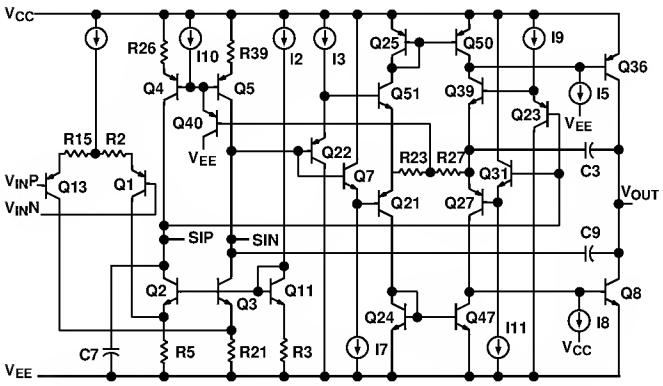


Figure 41. AD8051/AD8052 Simplified Schematic

APPLICATIONS

Layout Considerations

The specified high speed performance of the AD8051/AD8052/AD8054 requires careful attention to board layout and component selection. Proper RF design techniques and low-parasitic component selection are necessary.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path. The ground plane should be removed from the area near the input pins to reduce the parasitic capacitance.

Chip capacitors should be used for the supply bypassing. One end should be connected to the ground plane and the other within 3 mm of each power pin. An additional large (4.7 μF to 10 μF) tantalum electrolytic capacitor should be connected in parallel, but not necessarily so close, to supply current for fast, large signal changes at the output.

The feedback resistor should be located close to the inverting input pin in order to keep the parasitic capacitance at this node to a minimum. Parasitic capacitance of less than 1 pF at the inverting input can significantly affect high speed performance.

Stripline design techniques should be used for long signal traces (greater than about 25 mm). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.

Active Filters

Active filters at higher frequencies require wider bandwidth op amps to work effectively. Excessive phase shift produced by lower frequency op amps can significantly impact active filter performance.

Figure 42 shows an example of a 2 MHz biquad bandwidth filter that uses three op amps of an AD8054. Such circuits are sometimes used in medical ultrasound systems to lower the noise bandwidth of the analog signal before A/D conversion. Please note that the unused amplifiers' inputs should be tied to ground.

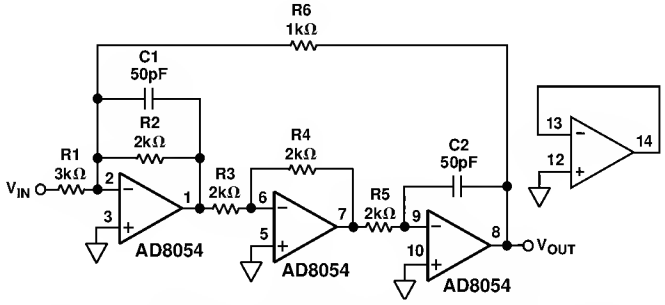


Figure 42. 2 MHz Biquad Bandpass Filter Using AD8054

The frequency response of the circuit is shown in Figure 43.

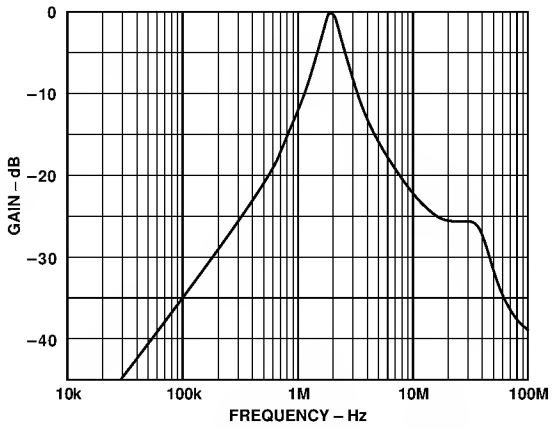


Figure 43. Frequency Response of 2 MHz Bandpass Biquad Filter

A/D and D/A Applications

Figure 44 is a schematic showing the AD8051 used as a driver for an AD9201, a 10-bit 20 MSPS dual A/D converter. This converter is designed to convert I and Q signals in communication systems. In this application, only the I channel is being driven. The I channel is enabled by applying a logic HIGH to SELECT, Pin 27.

The AD8051 is running from a dual supply and is configured for a gain of +2. The input signal is terminated in 50 Ω and

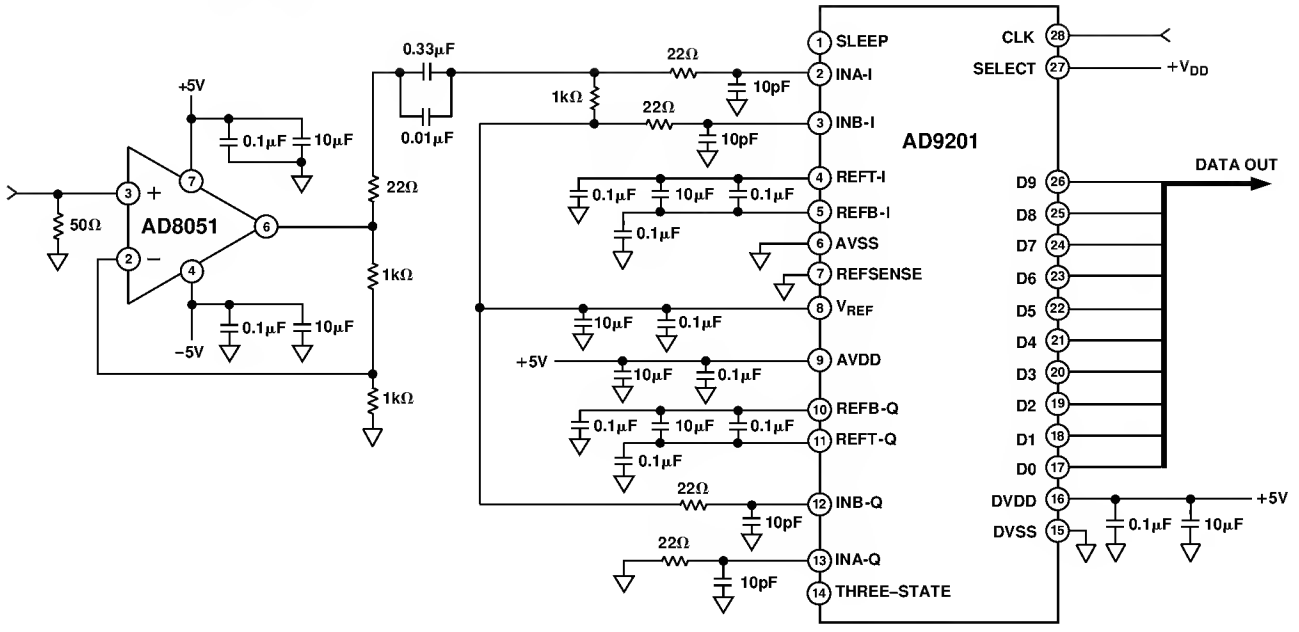


Figure 44. AD8051 Driving an AD9201, a 10-Bit 20 MSPS A/D Converter

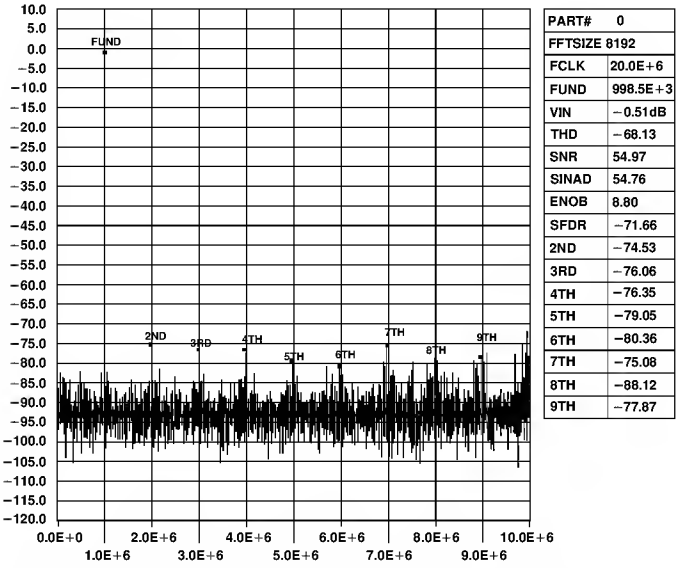
applied to the noninverting input of the AD8051. The amplifier output is 2 V p-p, which is the maximum input range of the AD9201. The 22 Ω series resistor limits the maximum current that flows and helps to lower the distortion of the A/D.

The AD9201 has differential inputs for each channel. These are designated the A and B inputs. The B inputs of each channel are connected to VREF (Pin 8) which supplies a positive reference of 2.5 V. Each of the B inputs has a small low pass filter that also helps to reduce distortion.

The output of the op amp is ac coupled into INA-I (Pin 2) via two parallel capacitors to provide good high frequency and low frequency coupling. The 1 kΩ resistor references the signal to VREF that is applied to INB-I. Thus, INA-I will swing both positive and negative with respect to the bias voltage applied to INB-I.

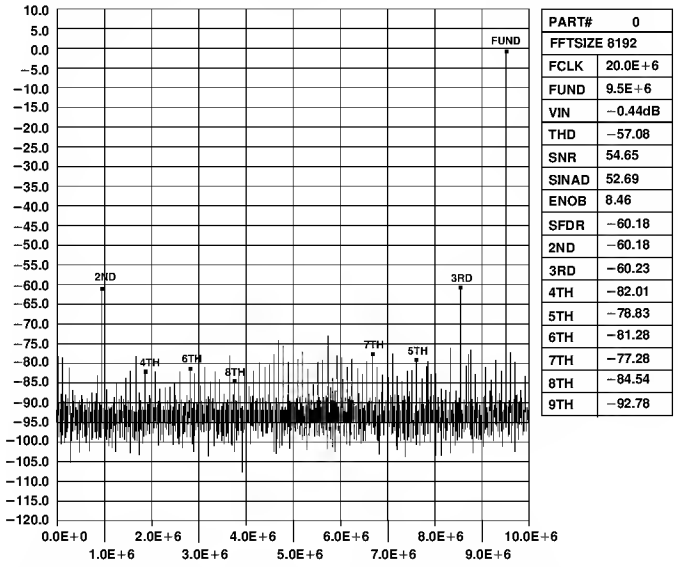
With the sampling clock running at 20 MSPS, the A/D output was analyzed with a digital analyzer. Two input frequencies were used, 1 MHz and 9.5 MHz, which is just short of the Nyquist frequency. These signals were well filtered to minimize any harmonics.

Figure 45 shows the FFT response of the A/D for the case of 1 MHz analog input. The SFDR is 71.66 dB and the A/D is producing 8.8 ENOB (effective number of bits). When the analog frequency was raised to 9.5 MHz, the SFDR was reduced to 60.18 dB and the A/D operated with 8.46 ENOBs as shown in Figure 46. The inclusion of the AD8051 in the circuit had no worsening of the distortion performance of the AD9201.



PART#	0
FFTSIZE	8192
FCLK	20.0E+6
FUND	998.5E+3
VIN	−0.51dB
THD	−68.13
SNR	54.97
SINAD	54.76
ENOB	8.80
SFDR	−71.66
2ND	−74.53
3RD	−76.06
4TH	−76.35
5TH	−79.05
6TH	−80.36
7TH	−75.08
8TH	−88.12
9TH	−77.87

Figure 45. FFT Plot for AD8051 Driving the AD9201 at 1 MHz



PART#	0
FFTSIZE	8192
FCLK	20.0E+6
FUND	9.5E+6
VIN	−0.44dB
THD	−57.08
SNR	54.65
SINAD	52.69
ENOB	8.46
SFDR	−60.18
2ND	−60.18
3RD	−60.23
4TH	−82.01
5TH	−78.83
6TH	−81.28
7TH	−77.28
8TH	−84.54
9TH	−92.78

Figure 46. FFT Plot for AD8051 Driving the AD9201 at 9.5 MHz

Sync Stripper

Synchronizing pulses are sometimes carried on video signals so as not to require a separate channel to carry the synchronizing information. However, for some functions, like A/D conversion, it is not desirable to have the sync pulses on the video signal. These pulses will reduce the dynamic range of the video signal and do not provide any useful information for such a function.

A sync stripper will remove the synchronizing pulses from a video signal while passing all the useful video information. Figure 47 shows a practical single supply circuit that uses only a single AD8051. It is capable of directly driving a reverse terminated video line.

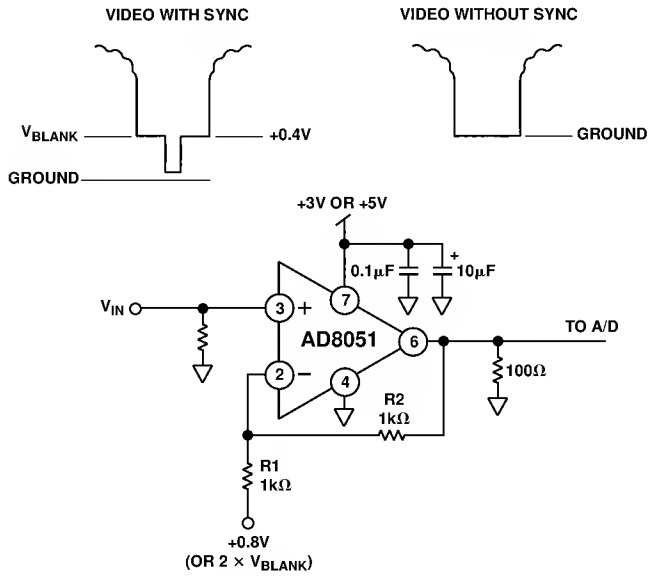


Figure 47. Sync Stripper

The video signal plus sync is applied to the noninverting input with the proper termination. The amplifier gain is set equal to two via the two 1 kΩ resistors in the feedback circuit. A bias voltage must be applied to R1 in order that the input signal has the sync pulses stripped at the proper level.

The blanking level of the input video pulse is the desired place to remove the sync information. This level is multiplied by two by the amplifier. This level must be at ground at the output in order for the sync stripping action to take place. Since the gain of the amplifier from the input of R1 to the output is –1, a voltage equal to $2 \times V_{BLANK}$ must be applied to make the blanking level come out at ground.

Single Supply Composite Video Line Driver

Many composite video signals have their blanking level at ground and have video information that is both positive and negative. Such signals require dual supply amplifiers to pass them. However, by ac level shifting a single supply amplifier can be used to pass these signals. The following complications may arise from such techniques.

Signals of bounded peak-to-peak amplitude that vary in duty cycle require larger dynamic swing capacity than their (bounded) peak to peak amplitude after they are ac coupled. As a worst case, the dynamic signal swing will approach twice the peak-to-peak value. The two conditions that define the maximum dynamic wing requirements are a signal that is mostly low, but goes high with a duty cycle that is a small fraction of a percent. The opposite condition defines the other extreme.

The worst case of composite video is not quite this demanding. One bounding condition is a signal that is mostly black for an entire frame, but has a white (full amplitude) minimum width spike at least once in a frame.

The other extreme is for a full white video signal. The blanking intervals and sync tips of such a signal will have negative-going excursions is compliance with the composite video specifications. The combination of horizontal and vertical blanking intervals limit such a signal to being at the highest (white) level for a maximum of about 75% of the time.

As a result of the duty cycles between the two extremes presented above, a 1 V p-p composite video signal that is multiplied by a gain of two requires about 3.2 V p-p of dynamic voltage swing at the output for an op amp to pass a composite video signal of arbitrary varying duty cycle without distortion.

Some circuits use a sync tip clamp to hold the sync tips at a relatively constant level in order to lower the amount of dynamic signal swing required. However, these circuits can have artifacts like sync tip compression unless they are driven by a source with a very low output impedance. The AD8051/AD8052/AD8054 have adequate signal swing when running on a single +5 V supply to handle an ac coupled composite video signal.

The input to the circuit in Figure 48 is a standard composite (1 V p-p) video signal that has the blanking level at ground. The input network level shifts the video signal by means of ac coupling. The noninverting input of the op amp is biased to half of the supply voltage.

The feedback circuit provides unity gain for the dc biasing of the input, and provides a gain of two for any signals that are in the video bandwidth. The output is ac coupled and terminated to drive the line.

The capacitor values were selected for providing minimum "tilt" or field time distortion of the video signal. These values would be required for video that is considered to be studio or broadcast quality. However, if a lower consumer grade of video, sometimes referred to as "consumer video" is all that is desired, the values and the cost of the capacitors can be reduced by as much as a factor of five with minimum visible degradation in the picture.

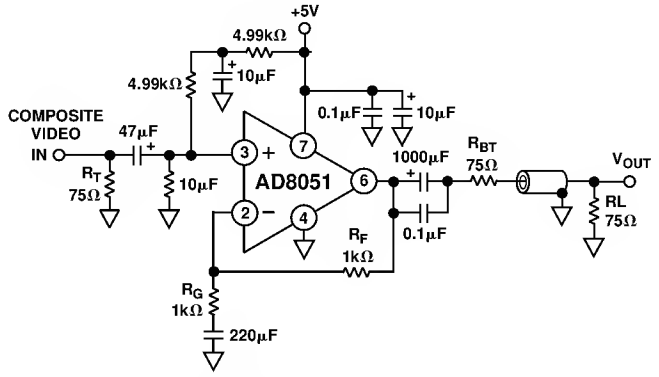
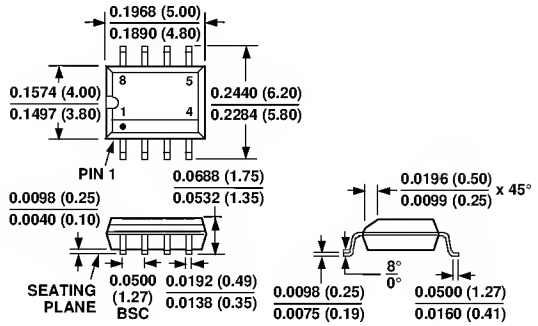


Figure 48. Single Supply Composite Video Line Driver

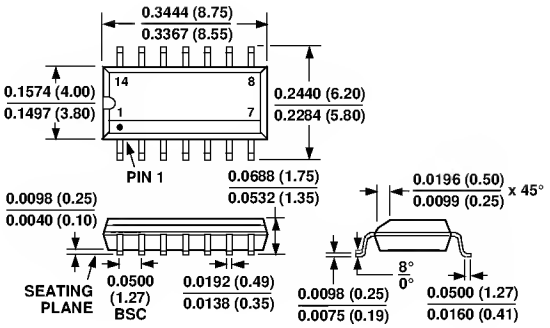
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

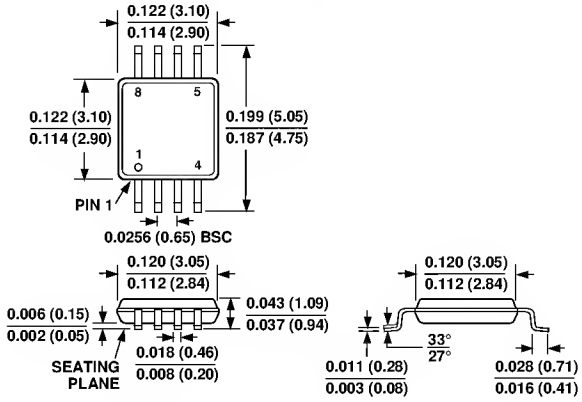
8-Lead SOIC (R-8)



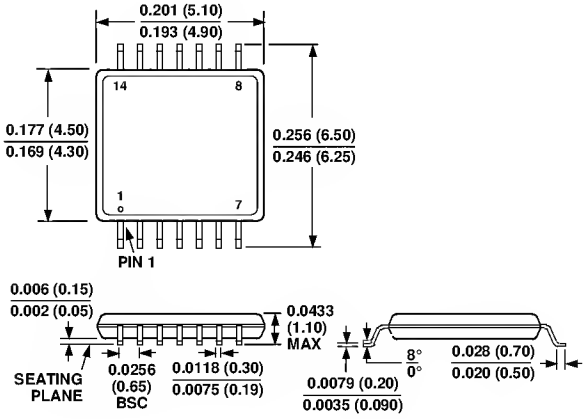
14-Lead SOIC (R-14)



8-Lead microSOIC (RM-08)



14-Lead TSSOP (RU-14)



5-Lead Plastic Surface Mount (RT-5)